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10/598,583	09/05/2006	Adrianus Josephus Bink	NL040236	7385

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EXAMINER	
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ART UNIT	PAPER NUMBER
2183	

NOTIFICATION DATE	DELIVERY MODE
04/10/2009	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

ip.department.us@nxp.com

Office Action Summary	Application No.	Applicant(s)	
	10/598,583	BINK ET AL.	
	Examiner	Art Unit	
	Jacob Petranek	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 January 2009*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-20 are pending.

2. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 1/29/2009 has been entered.

3. The office acknowledges the following papers:

Claims and arguments filed on 1/29/2009.

Withdrawn Objections and Rejections

4. The claim objection for claim 1 has been withdrawn due to amendment.

Claim objections

5. Claims 1-20 are objected to for the following reasons.

6. Claims 2-12 recite "an electronic circuit" in line 1 that should be changed to "[[an]] The electronic circuit" for proper antecedent basis.

7. Claim 1 recites "the pipeline stages" in line 4 that should be changed to "the first and second pipeline stages" for proper antecedent basis.

8. Claims 5 and 15 recite "an instruction of the third type" in lines 1-2 that should be changed to "[[an instruction of]] the third type of instruction" for proper antecedent basis.

9. Claims 6 and 16 recite "the instruction of the third type" in lines 1-2 that should be changed to "[[the instruction of]] the third type of instruction" for proper antecedent basis.

10. Claims 6 and 16 recites "the second or third type" in lines 3-4 that should be changed to "the second type of instruction or the third type of instruction" for proper antecedent basis.

11. Claims 7 and 17 recite "an instruction of the first type" in line 2 that should be changed to "[[an instruction of]] the first type of instruction" for proper antecedent basis.

12. Claims 14-20 recite "A method as claimed" in line 1 that should be changed to "[[A]] The method as claimed" for proper antecedent basis.

13. Claim 13 recites "the stages" in line 4 that should be changed to "the first and second pipeline stages" for proper antecedent basis.

New Claim Rejections - 35 USC § 112

14. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

15. Claims 1-20 are rejected under 35 U.S.C. §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 1 recites "each pipeline stage generating pipeline data." It's unclear if each pipeline stage is meant to be interpreted as each pipeline stage in the processor or if each pipeline stage is referring to the claimed first and second pipeline stages. For

examination purposes, the limitation will be interpreted as "each of the first and second pipeline [[stage]] stages generating pipeline data."

16. Claim 3 recites the limitation "the mode of operation" in line 2 of the claim. There is insufficient antecedent basis for this limitation in the claim.

17. Claim 6 and 16 recite the limitation "the following instruction" in line 3 of the claim. There is insufficient antecedent basis for this limitation in the claim.

18. Claim 13 recites the limitation "the instruction" in line 11 of the claim. There is insufficient antecedent basis for this limitation in the claim.

19. Claim 14 recites the limitation "the step of controlling" in lines 1-2 of the claim. There is insufficient antecedent basis for this limitation in the claim.

20. Claims 15-17 recites the limitation "the step of operating" in lines 1-2 of the claim. There is insufficient antecedent basis for this limitation in the claim.

21. Claims 2, 4-5, 7-12, and 18-20 are rejected due to their dependency.

New Claim Rejections - 35 USC § 103

22. The following is a quotation of 35 U.S.C. §103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

23. Claims 1-20 are rejected under 35 U.S.C. §103(a) as being unpatentable over Hennessy et al. ("Computer Organization and Design: The Hardware/Software Interface"), in view of Colwell et al. (U.S. 5,604,878).

24. As per claim 1:

Hennessy disclosed an electronic circuit adapted to process a plurality of types of instruction, the electronic circuit comprising:

first and second pipeline stages, each pipeline stage generating pipeline data (Hennessy: Figure 6.25, pipeline stages MEM and WB)(The pipeline stages of the processor generate data.);

a latch positioned between the pipeline stages (Hennessy: Figure 6.25, MEM/WB pipeline register)(It's obvious to one of ordinary skill in the art that the pipeline register can be implemented as a latch.); and

said electronic circuit being controlled to operate in a normal mode when processing a first type of instruction in which the latch is opened and closed in response to an enable signal (Hennessy: Figures 6.32 and 6.33, load instruction)(The MEM/WB pipeline register is opened and closed by the inherent clock signal of the processor not shown, which is the enable signal.), and;

wherein the first type of instruction requires processing by the first and second pipeline stages (Hennessy: Figures 6.32 and 6.33, load instruction)(The load instruction requires processing by the MEM and WB stages.) and the second type of instruction requires processing by the second pipeline stage (Hennessy: Figure 6.33, sub instruction)(The subtraction instruction requires processing by the WB stage.).

Hennessy failed to teach wherein the electronic circuit is controlled by a control signal based on a latency period of each respective instruction of said plurality of types of instruction and a reduced mode including a truncated passage when processing a

second type of instruction in which the enable signal is overridden by the control signal so that the latch is held open for the generated pipeline data to propagate, independent of the enable signal through the latch.

However, Colwell disclosed the electronic circuit is controlled by a control signal based on a latency period of each respective instruction of said plurality of types of instruction (Colwell: Figure 3 element 62, column 7 lines 55-67 continued to column 8 lines 1-3)(Hennessy: Figure 6.33, sub instruction)(The combination uses elements 61-62 to bypass the MEM/WB pipeline register when a writeback contention will be avoided. The control logic outputs a control signal based on a latency period of an instruction being executed when writeback contention can be avoided.),

a reduced mode including a truncated passage when processing a second type of instruction in which the enable signal is overridden by the control signal so that the latch is held open for the generated pipeline data to propagate, independent of the enable signal through the latch. (Colwell: Figure 3 elements 60-62, column 7 lines 55-67 continued to column 8 lines 1-3)(Hennessy: Figure 6.33, sub instruction)(The combination uses elements 61-62 to bypass the MEM/WB pipeline register when a writeback contention will be avoided. The control signal is the signal from element 62 that allows for two pipeline stages to affectively become a single stage, which overrides the clock signal of the MEM/WB pipeline register.).

The advantage of bypassing an extra pipeline stage that isn't needed for instructions is that these instructions will be allowed to retire earlier and result in increased performance when there is no writeback contention (Colwell: Column 2 lines

65-67 continued to column 3 lines 1-9). One of ordinary skill in the art would have been motivated to modify Hennessy to perform the pipeline stage bypassing of Colwell for the advantage above. Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to implement the pipeline stage bypassing of Colwell into the processor of Hennessy for the advantage of increasing performance of the processor of Hennessy.

25. As per claim 2:

Hennessy and Colwell disclosed an electronic circuit as claimed in claim 1, further comprising a latch control circuit connected to the latch, the latch control circuit being adapted to control the latch with the enable signal when the electronic circuit is in the normal mode (Hennessy: Figures 6.32 and 6.33, load instruction)(The MEM/WB pipeline register is opened and closed by the inherent clock signal of the processor not shown, which is the enable signal. The clock signal is part of the processor control unit.), and to hold the latch open when the electronic circuit is in the reduced mode (Colwell: Figure 3 elements 60-62, column 7 lines 55-67 continued to column 8 lines 1-3)(Hennessy: Figure 6.33, sub instruction)(The combination uses elements 61-62 to bypass the MEM/WB pipeline register when a writeback contention will be avoided, which are the control signals to control the pipeline register.).

26. As per claim 3:

Hennessy and Colwell disclosed an electronic circuit as claimed in claim 2, wherein the latch control circuit receives the control signal indicating the mode of operation of the electronic circuit (Colwell: Figure 3 elements 60-62, column 7 lines 55-

67 continued to column 8 lines 1-3)(The control logic generates a signal that determines the mode of the processor when Hennessy is acting as a 4 or 5 stage pipeline.).

27. As per claim 4:

Hennessy and Colwell disclosed an electronic circuit as claimed in claim 1, wherein the electronic circuit is adapted to process a third type of instruction, wherein the third type of instruction does not require processing by the second pipeline stage (Hennessy: Figures 6.26 and 6.28, pages 466 and 468, store and branch instructions)(Store and branch instructions don't write to the register file, which is the second pipeline stage, as shown by the control signals in figure 6.28.).

28. As per claim 5:

Hennessy and Colwell disclosed an electronic circuit as claimed in 4, wherein the electronic circuit is adapted to operate in the normal mode until an instruction of the third type is processed (Hennessy: Figures 6.31-6.34)(The processor acts in a normal mode of processing where instructions are processing in 5 stages.).

29. As per claim 6:

Hennessy and Colwell disclosed an electronic circuit as claimed in claim 5, wherein, after the instruction of the third type is processed, the electronic circuit is adapted to operate in the reduced mode if the following instruction is of the second or third type (Hennessy: Figure 6.26, page 466 and 468, store and branch instructions)(Colwell: Figure 3 elements 60-62, column 7 lines 55-67 continued to column 8 lines 1-3)(When a store instruction is processed, it doesn't write to the register file in the fifth stage, which allows a preceding instruction to write to the register file in

the fourth pipeline stage by utilizing the bypass of Colwell. This results in changing the processor to a reducing mode. It's inherent that the bypass can not be utilized if the preceding instruction is a load instruction that must write to the register file in the fifth pipeline stage in the pipelined processor of Hennessy that issued a single instruction per cycle and has a single writeback port on the register file.).

30. As per claim 7:

Hennessy and Colwell disclosed an electronic circuit as claimed in claim 4, wherein the electronic circuit is adapted to operate in the reduced mode until an instruction of the first type is processed (Hennessy: Figure 6.26, page 466 and 468, store and branch instructions)(Colwell: Figure 3 elements 60-62, column 7 lines 55-67 continued to column 8 lines 1-3)(When a store instruction is processed, it doesn't write to the register file in the fifth stage, which allows a preceding instruction to write to the register file in the fourth pipeline stage by utilizing the bypass of Colwell. This results in changing the processor to a reducing mode. It's inherent that the bypass can be utilized until a load instruction is executed, which must write to the register file in the fifth pipeline stage.).

31. As per claim 8:

Hennessy and Colwell disclosed an electronic circuit as claimed in claim 1, wherein the first type of instruction includes a load instruction (Hennessy: Figure 6.26)(The load instruction is the first type of instruction.).

32. As per claim 9:

Hennessy and Colwell disclosed an electronic circuit as claimed in claim l, wherein the second type of instruction includes an arithmetic computation instruction (Hennessy: Figure 6.26)(The add and sub instructions are the second type of instructions.).

33. As per claim 10:

Hennessy and Colwell disclosed an electronic circuit as claimed in claim 4, wherein the third type of instruction includes compare, store, branch and jump instructions (Hennessy: Figure 6.26)(The store and branch instructions are the third type of instructions. Official notice is given that jump and compare instructions don't write results to the register file. Thus, it's obvious to one of ordinary skill in the art to include jump and compare instructions in the processor of Hennessy as the third type of instructions.).

34. As per claim 11:

Hennessy and Colwell disclosed an electronic circuit as claimed in claim 1, wherein the first pipeline stage comprises a data memory (Hennessy: Figure 6.25, MEM pipeline stage.).

35. As per claim 12:

Hennessy and Colwell disclosed an electronic circuit as claimed in any claim 1, wherein the second pipeline stage comprises a write back stage (Hennessy: Figure 6.25, WB pipeline stage.).

36. As per claim 13:

Claim 13 essentially recites the same limitations of claim 1. Therefore, claim 13 is rejected for the same reasons as claim 1.

37. As per claim 14:

The additional limitation(s) of claim 14 basically recite the additional limitation(s) of claim 4. Therefore, claim 14 is rejected for the same reason(s) as claim 4.

38. As per claim 15:

The additional limitation(s) of claim 15 basically recite the additional limitation(s) of claim 5. Therefore, claim 15 is rejected for the same reason(s) as claim 5.

39. As per claim 16:

The additional limitation(s) of claim 16 basically recite the additional limitation(s) of claim 6. Therefore, claim 16 is rejected for the same reason(s) as claim 6.

40. As per claim 17:

The additional limitation(s) of claim 17 basically recite the additional limitation(s) of claim 7. Therefore, claim 17 is rejected for the same reason(s) as claim 7.

41. As per claim 18:

The additional limitation(s) of claim 18 basically recite the additional limitation(s) of claim 8. Therefore, claim 18 is rejected for the same reason(s) as claim 8.

42. As per claim 19:

The additional limitation(s) of claim 19 basically recite the additional limitation(s) of claim 9. Therefore, claim 19 is rejected for the same reason(s) as claim 9.

43. As per claim 20:

The additional limitation(s) of claim 20 basically recite the additional limitation(s) of claim 10. Therefore, claim 20 is rejected for the same reason(s) as claim 10.

Response to Arguments

44. The arguments presented by Applicant in the response, received on 1/29/2009 are not considered persuasive.

45. Applicant argues "Moreover, it does not make sense to place the extension mechanism in any other location because the stated purpose of these components is to delay the output of the pipeline for a clock cycle. As such, were the skilled artisan to implement the teachings of Colwell into the pipeline stage of Hennessy, the teachings would be implemented in a manner that would not conform to the claim limitations directed to the latching being located between two pipeline stages" for claim 1.

This argument is not found to be persuasive for the following reason. The pipe extend buffer extends the instructions execution time by a single clock cycle. Thus, the pipe extend buffer is equivalent to any of the pipeline registers shown in figure 6.25 of Hennessy. The placement of the pipe extend buffer and the MUX element 61 of Colwell anywhere in Hennessy would read upon a latch being positioned between two pipeline stages.

46. Applicant argues "Moreover, the Office Action has misinterpreted the teachings of at least the Colwell reference with regards to overriding of an enable signal and thereby fails to show correspondence to related limitations. The Office Action equates a clock signal (incorrectly identified as inherent)[1] to an enable signal. In no manner,

however, does Colwell teach that such an enable signal is overridden by the control signal. Instead, Colwell teaches that the control signal controls multiplexer 61 to selectively provide either the input of buffer 60 or the output of buffer 60. Thus, the control signal does not change the functionality of buffer 60 because, regardless of the control signal, data is still saved in buffer 60. For example, if the output of pipeline stage 3 has a value "A", this value A is passed to both buffer 60 and multiplexer 61. Multiplexer 61 responds to the control signal by sending value A to bus 120 either immediately or after being stored in buffer 60; however, the value A is still stored in buffer 60 regardless of the control signal. Thus, the enable signal is not overridden by the control signal" for claim 1.

This argument is not found to be persuasive for the following reason. Clock signals are inherent within a synchronous pipeline processor, which is shown by Hennessy in figure 6.25. The combination results in placing MUX element 61 in the writeback stage after the MEM/WB pipeline register. Thus, an arithmetic instruction executed by the ALU has the option of writing back to the register file in the MEM stage or the WB stage of Hennessy based on the output of the control logic element 62 in Colwell. When the control logic determines that an arithmetic instruction can write to the register file in the MEM stage, the control signal allowing the instruction's data to pass through MUX element 62 bypasses the clock signal on the MEM/WB stage. This control signal overrides the clock signal for the instruction because the instruction would normally have written it's execution results back to the register file in the WB stage by

the clock signal clocking the MEM/WB pipeline register. Thus, the clock signal is overridden by the control signal allowing for early retirement.

47. Applicant argues "Applicant further submits that the teachings of the Hennessy and Colwell references would lead the skilled artisan away from any combination that corresponds to the claim limitations" for claim 1.

This argument is not found to be persuasive for the following reason. A reference "teaches away" when it states that something cannot be done. See In re Gurley, 27 F.3d 551, 553, 31 USPQ2d 1130, 1130 (Fed. Cir. 1994).

48. Applicant argues "Moreover, adding the additional pipe extend buffer 60 only serves to delay execution times of the pipeline, thereby avoiding contention with another pipeline. Thus, the skilled artisan would not look to the teachings of Hennessy and Colwell references to implement a delay the pipeline of Hennessy that addresses a nonexistent contention problem and only serves to slow the pipeline processing. As such, the references teach away from the asserted combination and the combination is not obvious" for claim 1.

This argument is not found to be persuasive for the following reason. The applicant is incorrectly interpreting the combination. The pipe extend buffer does not add another pipeline stage to Hennessy. Instead, the pipe extend buffer is equivalent to the MEM/WB pipeline register. The combination only adds the functionality of arithmetic instructions to bypass the MEM/WB pipeline register via MUX element 61 for early retirement.

49. Applicant argues "The reason for the proposed modification is to obtain the "advantage of bypassing an extra pipeline stage that isn't needed for instructions". *See,* Instant Office Action at page 5. The proposed modification, however, does not bypass an "extra pipeline stage." Rather, as discussed above, Colwell teaches that the purpose of the pipe extend buffer 60 and MUX 61 is to effectively delay the pipeline. As such, the reason presented for the modification is based upon an incorrect interpretation of how the combination would function *(e.g.,* incorrectly asserting increased speed when the combination would decrease speed). Thus, the modification would not achieve the stated benefit of bypassing a pipeline stage" for claim 1.

This argument is not found to be persuasive for the following reason. The applicant is incorrectly interpreting the combination. The pipe extend buffer does not add another pipeline stage to Hennessy. Instead, the pipe extend buffer is equivalent to the MEM/WB pipeline register. The combination only adds the functionality of arithmetic instructions to bypass the MEM/WB pipeline register via MUX element 61 for early retirement. Therefore, the combination benefits as specified in the motivation.

Conclusion

The following is text cited from 37 CFR 1.111(c): In amending in reply to a rejection of claims in an application or patent under reexamination, the applicant or patent owner must clearly point out the patentable novelty which he or she thinks the claims present in view of the state of the art disclosed by the references cited or the

objections made. The applicant or patent owner must also show how the amendments avoid such references or objections.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jacob Petranek whose telephone number is 571-272-5988. The examiner can normally be reached on M-F 8:00-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/Jacob Petranek/
Examiner, Art Unit 2183